IN THE DRAWINGS:

The attached sheet of drawing includes changes to FIG. 2. This sheet replaces the original sheet of FIG. 2. FIG. 2 has been amended by labeling Propagate/Generate block (now shown as block "210") to conform to the specification as suggested by the Examiner.

Attachment: Replacement Sheet (FIG. 2)

REMARKS

1. Introduction

Claims 10-25 and 32-42 are pending in this application. (Claims 1-9 and 26-31 have been withdrawn.) In the last Office Action, the drawings were objected to because of a typographical error in FIG. 2, and claims 12 and 33 were rejected under 35 U.S.C. § 112, ¶ 1 as being indefinite. Claims 10, 13, 17 and 19 were rejected as anticipated by Ware (U.S. Pat. No. 4,623,982), and claims 14, 22-25, 32, 34-35, 37, and 40-41 were rejected as obvious over Ware. Claims 10, 12-14, 17, 19, 22-25, 32, 34-35, 37 and 40-41 were rejected as obvious in view of Levin (U.S. Pat. No. 4,118,786). Claims 11 and 18 were rejected either as obvious over Levin in view of Vo (U.S. Pat. No. 4,737,926) or as obvious over Ware in view of Vo.

Finally, claims 15-16, 20-21, 33, 36, 38-39, and 42 were objected as dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including the limitations of the base claims. Claim 33 was indicated to be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112, ¶ 1. Applicant appreciates this indication of allowability.

This Response amends claim 10 to clarify the language without changing the scope of this claim and amends the specification for clarity.

2. The informality in FIG. 2 has been corrected

FIG. 2 has been amended by labeling Propagate/Generate block (now shown as block "210") to conform to the specification as suggested by the Examiner. A replacement figure is enclosed. Applicant respectfully requests that the Examiner withdraw the objection to this figure.

3. Claims 12 and 33 are believed to be definite

In rejecting claims 12 and 33 under 35 U.S.C. § 112, ¶ 1, the last Office Action requested clarification of the phrase "intermediate XOR value" as used in these claims. *See* Office Action, at pages 2-3. In this regard, Applicant notes that the specification states the following at page 10, lines 4-8 (emphasis added):

> "According to the embodiment shown in FIG. 3, the intermediate values A_i XOR B_i (which are XOR'ed with the value $carry_i$ to provide the values Sum_i) is provided by a NAND tree, such as a NAND gate connected to one or more buffers at the inputs and/or output, rather than by an XOR gate. For example, the value A_1 XOR B_1 is provided by inverting the output of NAND gate 314."

Thus, the value "A_1 XOR B_1" shown in FIG. 3 is based upon the propagate value P_1 and generate value G_1. As shown in FIG. 3, this value is not provided by an XOR gate.

In addition, the specification states the following at page 1, lines 19-23 (emphasis added):

> "As is known in the art, a carry look-ahead adder may include sub-circuits that provide intermediate values such as a generate value, a propagate value, and a carry value for different bit positions in the binary numbers being added. Such generate, propagate and carry values may then be used to provide the final sums bits."

In FIG. 3, the value "A_1 XOR B_1" is an "intermediate XOR value" because it is not the final output of Adder 100. Rather, A_1 XOR B_1 is an input to Final XOR block 161, which as shown in FIG. 1 outputs a final value Sum_1 from Adder 100.

In view of this description from the specification, Applicant respectfully suggests that the language of claims 12 and 33 is definite, and Applicant requests withdrawal of the rejection of these claims under 35 U.S.C. § 112, ¶ 1.

4. Claims 10-25 are believed to be patentable over Ware and Levin

Applicant submits that claims 10-25 are patentable over Ware, Levin and the other art of record. Among other things, neither Ware nor Levin discloses a method that includes "determining a carry-out value for each propagate value based at least in part on the propagate value and corresponding generate value, wherein the carry-out values are determined by a plurality of carry generation blocks, and wherein one of the carry generation blocks determines exactly three of the carry-out values" as recited in claim 10 (emphasis added). In addition, neither Ware nor Levin discloses a look-ahead carry adder circuit comprising "a plurality of carry generation blocks each having inputs connected to two or more of said propagate outputs and two or more of said generate outputs, wherein one of the carry generation blocks is connected to exactly three of the propagate outputs and three of the generate outputs, and wherein each of the carry generation blocks has a plurality of carry outputs" as recited in claim 17 (emphasis added).

The last Office Action rejected claims 10 and 17 as anticipated by Ware. *See* Office Action, page 3. In order for a reference to anticipate a claim, the reference must teach every element of the claim. *See* MPEP 2131. In rejecting claims 10 and 17 as anticipated by Ware, the last Office Action acknowledges that "Ware does not specifically detail the claimed 'one of the carry generation blocks determine exactly **three** of the carry-output values'". *See* Office Action, page 3 (emphasis in original). Thus, the last Office Action acknowledges that Ware does not teach every element of claim 10. The last Office Action applies a "similar rationale" for rejecting claim 17. Because Ware does not teach every limitation of claims 10 and 17, as acknowledged in the last Office Action, the rejection of these claims as anticipated by Ware should be withdrawn.

The last Office Action also rejects claims 10 and 17 "under 35 U.S.C. 103(a) as being unpatentble over Levin et al." *See* Office Action, page 4. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *See* MPEP 2143.03. As to claim 10, the last Office Action

acknowledges that "Levin et al. do NOT specifically detail the claimed 'one of the carry generation blocks determine exactly **three** of the carry-output values'". *See* Office Action, page 4 (emphasis in original). In this regard, the last Office Action states that "the size of block is obvious design choice for the logic designer, e.g., Persoon (US Pat. 5,117,386) or Ware (US Pat. 4,623,982), disclose parallel adders having THREE-bit adder(s)." *Id.* (emphasis in original). The last Office Action states that claim 17 is rejected under a "similar rationale." See Office Action, at 5.

As a technical matter, Applicant notes that, if the Office Action is to rely upon Persoon or Lo as teaching the missing limitation, Persoon or Lo should formally be part of a multi-reference rejection, as was the case with the rejection of claim 11 on page 8 of the Office Action.

More importantly, Applicant submits that even to the extent that Persoon and Ware do "disclose parallel adders having THREE-bit adder(s)," as stated in the last Office Action, these references do not disclose a plurality of carry-generation blocks "wherein one of the carry generation blocks determines exactly three of the carry-out values" as recited in claims 10 or a plurality of carry-generation blocks "wherein one of the carry generation blocks is connected to exactly three of the propagate outputs and three of the generate outputs" as recited in claim 17. In other words, claims 10 and 17 do not recite three-bit adders; this is not a limitation of these claims. The fact that Persoon and Ware do not disclose a carry generation block that determines exactly three of the carry-out values, which is a limitation of claim 10, is confirmed on page 3 of the last Office Action, which acknowledges that Ware does not disclose this limitation.

Just as importantly, "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." *See* MPEP 2103.01 (emphasis added). Merely labeling a claim limitation as a "design choice" is of no consequence in the obviousness analysis and cannot substitute for the required teaching, suggestion or motivation. If "design

choices" were always obvious, then no invention would be patentable because every invention is the inventor's choice of that particular design. Because the last Office Action fails to even identify some teaching suggestion or motivation to combine or modify the references, the rejection of claims 10 and 17 as obvious should be withdrawn. Finally, Applicant notes that to reject a claim as obvious, the Office Action must provide "actual evidence" that there would have been a suggestion to combine the references. *See, e.g., In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

For at least these reasons, claims 10 and 17 are believed to be patentable. Claims 11-16 and 18-25 depend from one of claims 10 or 17 and are patentable for at least the same reason as claims 10 or 17, as well as for additional limitations contained therein, which Applicant declines to separately discuss at this time.

5. Claims 32-36 are believed to be patentable over Ware and Levin

Applicant submits that claims 32-36 are patentable over Ware, Levin and the other art of record at least because neither Ware nor Levin discloses a method of adding two multi-bit addends that includes "determining a carry-out value for each propagate value based at least in part on the propagate value and corresponding generate value, wherein the carry-out values are determined by a plurality of carry generation blocks that include a plurality of tapered transistor stacks" as recited in claim 32 (emphasis added).

In rejecting claim 32 as obvious over Levin, the last Office Action notes that "Levin et al do NOT specifically detail the claimed 'carry generation blocks that include a plurality of **tapered transistor stacks**" feature; however, "**tapered transistor stacks** is a broad term [by definition]." *See* Office Action at 7 (emphasis in original). In rejecting claim 32 as obvious over Ware, the last Office Action refers to the rejection of claim 14, which states: "the examiner believes that the '**tapered transistor stacks**' feature is old and well known in the art. For example, a simple and/or combination logic gate could be implemented by such feature, e.g., a two-input CMOS AND gate can be

implemented by '**tapered transistor stacks**'. Also see Gonfaus et al (Figs. 2-4)." *See* Office Action, pages 7-8.

Applicant notes that FIGS. 7 and 8 of the present application show AND-OR-INVERT gate 309 with tapered stacks. *See* Specification at page 3, lines 10-14. The tapered aspect of the stacks shown is discussed generally at pages 20-23 of the specification. As to FIG. 7, the specification states specifically at page 21, lines 19-24 (emphasis added) that:

> "This embodiment contains a number of transistor stacks which are connections from a voltage supply to an output. One stack in AND-OR-INVERT gate 431 is transistor 701 and transistor 702 (to output 710). Another is transistor 701 to 705, and another is transistor 704 to 703. In an embodiment, the stacks are tapped so that the transistor closer to the output is smaller."

Note that, as shown above, this Response amends this paragraph to correct obvious typographical errors.

As noted above, claim 32 requires "carry generation blocks" that include a plurality of "tapered transistor stacks." Applicant submits that, pursuant to the specification (quoted above), the meaning of the term "tapered transistor stacks" requires that the stack have a smaller transistor closest to the output. Applicant submits that the use of a transistor stack with a smaller transistor closest to the output in a carry generation block is not "old and well known in the art." Applicant does not believe that Gonfaus et al (Figs. 2-4) disclose the use of a transistor stack with a smaller transistor closest to the output. Moreover, even if Gonfaus or some other reference disclosed a transistor stack with a smaller transistor closest to the output, and even if "a simple and/or combination logic gate *could be* implemented by such feature," as stated in the last Office Action at page 5 (emphasis added), there is no evidence of a motivation to use such a feature in a carry generate block as recited in claim 32.

For at least these reasons, claim 32 is believed to be patentable. Claims 33-36 depend from claim 32 and are patentable for at least the same reason as claims 32, as

well as for additional limitations contained therein, which Applicant declines to separately discuss at this time.

6. Claims 37-42 are believed to be patentable over Ware and Levin

Applicant submits that claims 37-42 are patentable over Ware, Levin and the other art of record at least because neither Ware nor Levin discloses a look-ahead carry adder circuit that includes "a plurality of carry generation blocks each having inputs connected to two or more of said propagate outputs and two or more of said generate outputs, wherein each of the carry generation blocks has a plurality of carry outputs, and wherein there is one critical path through the plurality of carry generation blocks" as recited in claim 37 (emphasis added).

The specification discusses "critical path" at page 3, line 1 to page 4, line 4 (emphasis added) as follows:

> "For an adder, the critical path is the slowest path from an input addend bit to a sum output bit and may be, for example, the path with the most logic or longest wires. The criticality of a path may be determined, for example, by simulation. In an embodiment of the present invention, the adder has only one critical path."

In rejecting claim 37 as obvious over Ware and as obvious over Levin, the last Office Action applied the rationale used to rejection claim 13. *See* Office Action at 6, 8. In rejecting claim 13, the last Office Action states that a "parallel adder circuit should have at least one critical path through the plurality of carry generation blocks." *See* Office Action at 5 (emphasis added).

Applicant submits that the last Office Action should be withdrawn because there is no evidence that either Ware, Levin or any other references discloses a single critical path though the plurality of carry generate gates as claimed. The fact that an adder circuit should have "at least one" critical path is not determinative because the claims recites only having a single critical path. This feature is not shown or suggested by the art of record.

For at least these reasons, claim 37 is believed to be patentable. Claims 38-42 depend from claim 37 and are patentable for at least the same reason as claims 37, as well as for additional limitations contained therein, which Applicant declines to separately discuss at this time.

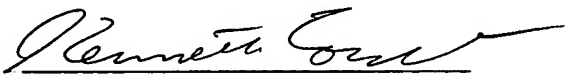
7. Conclusion

Applicant respectfully requests entry of the above amendments and favorable action in connection with this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. 1.16 or 1.17 to Kenyon & Kenyon Deposit Account No. 11-0600. The Examiner is invited to contact the undersigned at (202) 220-4310 to discuss any matter concerning this application.

Respectfully submitted,

Kenyon & Kenyon

Date: March 15, 2005



Kenneth R. Corsello
Registration No. 38,115
(Attorney for Intel Corporation)

KENYON & KENYON
1500 K Street, N.W.
Washington, D.C. 20005
Ph.: (202) 220-4200
Fax.: (202) 220-4201